In The Claims:

Please amend the claims as follows:

1. (Currently Amended) A fault tolerant processing circuit 18 comprising:

at least three homogenous processor groupings 20 each of said at least three processor groupings 20 having a plurality of processor grouping inputs and a plurality of processor grouping outputs;

a processor system clock coupled to the fault tolerant processing circuit;

a synchronizing circuit 21 comprising a plurality of output synchronizers, each output synchronizer in operative communication with a corresponding respective processor grouping for synchronizing the output of each processor grouping;

a logic circuit in operative communication with said synchronizing circuit 21, said logic circuit comprising a fault detection circuit and a fault mask circuit, said logic circuit adapted to compare said plurality of processor group outputs to detect errors in any one of said plurality of processor group outputs through selecting bits from said processor group outputs, wherein bit selection is generated as a function of whether a first one of said plurality of processor group outputs is synchronous or asynchronous, wherein at least one of said plurality of processor group outputs is asynchronous; and

a control logic circuit for resetting each of said at least three processor groups when none of said at least three processor groups is in a majority of said processor groups, wherein said fault mask circuit is adapted to mask the output of a respective processor grouping associated with a detected error and signal a detected error.

2. (Original) A fault tolerant processing system 18 according to claim 1 wherein said synchronizing circuit 21 further comprises continuously active synchronization signals.

3. (Original) A fault tolerant processing system 18 according to claim 1 wherein said synchronizing circuit 21 further comprises periodically active synchronization signals.

4. (Cancelled)

5. (Original) A fault tolerant processing system 18 according to claim 1 wherein said synchronizing circuit 21 further comprises logic operative to synchronize a JTAG TCLK with said processor system clock.

6. (Original) A fault tolerant processing system 18 according to claim 1 wherein an expected rate of transient faults is tuned by a latent fault scrubbing rate.

7. (Previously Presented) A fault tolerant processing system 18 according to claim 1 wherein said at least three processor groupings 20 comprises:

a central processing unit (CPU) 24, having an operating step executed during a clock cycle and operating synchronously with each other CPU 24, each operating step of each CPU 24 being accomplished in parallel and substantially simultaneously with each of the other at least three CPUs 24 each clock cycle, each of said at least three CPUs 24 having a plurality of CPU inputs and a plurality of CPU outputs; and

a respective support logic device coupled to said plurality of CPU inputs and said plurality of CPU outputs and having a plurality of support logic device inputs and outputs coupled to said respective CPU 24.

8. (Previously Presented) A fault tolerant processing system 18 according to claim 1, wherein said logic circuit resets each of said at least three processor groups upon detecting a fault and, in response, each of said at least three processor groups restart at a hardware defined operating step.

9. (Original) A fault tolerant processing system according to claim 8, wherein said logic circuit interrupts said at least three processor groups when one of said processor groups has a fault, whereby each of said at least three processor groups without detected faults store state information and said logic circuit resets each of said at least three processor groups after said state information is stored to restart said at least three processor groups at a state defined operating step.

10. (Original) A fault tolerant processing system 18 according to claim 8, wherein said logic circuit interrupts said at least three processor groups when a minority of said processor groups has a fault, and wherein each of said at least three processor groups without an error stores state information and said logic circuit resets each of said at least three processor groups after said state information is stored to restart said at least three processor groups at a state defined operating step.

11. (Original) A fault tolerant processing system 18 according to claim 9, wherein said logic circuit includes fault control and status registers for storing said state information.

12. (Previously Presented) A fault tolerant processing system 18 according to claim 1, wherein each of said at least three processor groupings includes a memory system.

13. (Previously Presented) A satellite system 10 comprising:

a ground station 14;

a satellite 12 in operative communication with said ground station 14, said satellite 12 including a fault tolerant processing circuit comprising:

at least three processor groupings 20 each of said at least three processor groupings 20 having a plurality of processor grouping inputs and a plurality of processor grouping outputs;

a synchronizing circuit 21 comprising a plurality of output synchronizers, each output synchronizer in operative communication with a corresponding respective processor grouping for synchronizing the output of each processor grouping;

a fault logic circuit 22 in operative communication with said synchronizing circuit 21, said fault logic circuit 22 comprising a fault detection circuit and a fault mask circuit, said fault logic circuit 22 adapted to compare said plurality of processor group outputs to detect errors in any one of said plurality of processor group outputs through selecting bits from said processor group outputs, wherein bit selection is generated as a function of whether a first one of said plurality of processor group outputs is synchronous or asynchronous and whether said first one of said plurality of processor group outputs is always valid or valid based on a state of a second one of said plurality of outputs;

a control logic circuit for resetting each of said at least three processor groups when none of said at least three processor groups is in a majority of said processor groups, wherein said fault mask circuit is adapted to mask the output of a respective processor grouping associated with a detected error and signal a detected error; and

a system bus coupled to each of said plurality of processor group inputs and said fault logic circuit output.

14. (Previously Presented) A fault tolerant processing circuit 18 according to claim 13 wherein said synchronizing circuit 21 further comprises continuously active synchronization signals.

15. (Previously Presented) A fault tolerant processing circuit 18 according to claim 13 wherein said synchronizing circuit 21 further comprises periodically active synchronization signals.

16. (Cancelled)

17. (Previously Presented) A fault tolerant processing circuit 18 according to claim 13 wherein said synchronizing circuit 21 further comprises logic operative to synchronize a JTAG TCLK with said processor system clock.

18. (Previously Presented) A fault tolerant processing circuit 18 according to claim 13 wherein an expected rate of transient faults is tuned by said latent fault scrubbing rate.

19. (Previously Presented) A satellite system 10 according to claim 13 wherein said at least three processor groupings 20 comprises:

a central processing unit (CPU), having an operating step executed during a clock cycle and operating synchronously with each other CPU 24, each operating step of each CPU 24 being accomplished in parallel and substantially simultaneously with each of the other at least three CPUs 24 each clock cycle, each of said at least three CPUs 24 having a plurality of CPU inputs and a plurality of CPU outputs; and

a respective support logic device coupled to said plurality of CPU inputs and said plurality of CPU outputs and having a plurality of support logic device inputs and outputs coupled to said respective CPU 24.

20. (Previously Presented) A satellite system 10 according to claim 13, wherein said fault logic circuit 22 resets each of said at least three processor groups upon detecting a fault and, in response, each of said at least three processor groups restart at a hardware defined operating step.

21. (Original) A satellite system 10 according to claim 15, wherein said fault logic circuit 22 interrupts said at least three processor groups when one of said processor groups has a fault, whereby each of said at least three processor groups without detected faults store state information and said fault logic circuit 22 resets each of said at least three processor groups after said state information is stored to restart said at least three processor groups at a state defined operating step.

22. (Original) A satellite system 10 according to claim 15, wherein said fault logic circuit 22 interrupts said at least three processor groups when a minority of said processor groups has a fault, and wherein each of said at least three processor groups without an error stores state information and said fault logic circuit 22 resets each of said at least three processor groups after said state information is stored to restart said at least three processor groups at a state defined operating step.

23. (Original) A satellite system 10 according to claim 21, wherein said fault logic circuit 22 includes fault control and status registers for storing said state information.

24. (Previously Presented) A satellite system 10 according to claim 13, wherein each of said at least three processor groupings includes a memory system.

25. (Previously Presented) A method of masking the effect of a single event upset in a fault tolerant processing system 18 including at least three processor groups, each processor group including a CPU 24, an input, an output, and a support logic device, said method comprising the steps of:

monitoring each of said plurality of processor group outputs;

detecting an error in one of said processor group outputs by comparing the outputs of each of said at three processor groups against each other through selecting bits from said processor group outputs, wherein bit selection is generated as a function of whether a first one of said plurality of processor group outputs is synchronous or asynchronous and whether said first one of said plurality of processor group outputs is always valid or valid based on a state of a second one of said plurality of processor group outputs;

classifying each processor group as a majority processor group or minority processor group, said majority processor groups all having equal value outputs and comprising

a majority of all processor groups, said minority processing groups each having an output different than each majority processing group;

when any processor group is classified as a minority processor group, storing state information for at least one of said processor groups classified as a majority processor group;

simultaneously resetting each of said processor groups to restart at a state defined operating step; and

restoring said stored state information to each of said processor groups.

26. (Original) A method according to claim 25 wherein, when no processor group is classified as a majority processor group, simultaneously resetting each of said processor groups and initializing each of said processor groups to restart at a state defined operating step.